3801

10-BIT SERIAL/PARALLEL-PARALLEL/SERIAL CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3801 is a monolithic MOS/LSI ten bit serial/parallel - parallel/serial converter utilizing P-Channel Enhancement mode MOS technology. The device has the capability of serial or parallel input and serial or parallel output. A holding register included on the chip is isolated from the shift register by transfer gates. In serial to parallel applications data may be stored in the holding register while new data is being entered into the shift register.

FEATURES

- **8 AND 10 BIT SERIAL OUTPUT**
- **250 kHz SERIAL TO PARALLEL OPERATION**
- **500 kHz PARALLEL TO PARALLEL OPERATION**
- **120 mW POWER DISSIPATION**
- **INPUT GATE PROTECTION**
- **SET AND RESET OF HOLDING REGISTER**
- **OUTPUT STROBE CONTROL**
- **SINGLE PHASE CLOCK**
- **RESET OF SERIAL REGISTER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

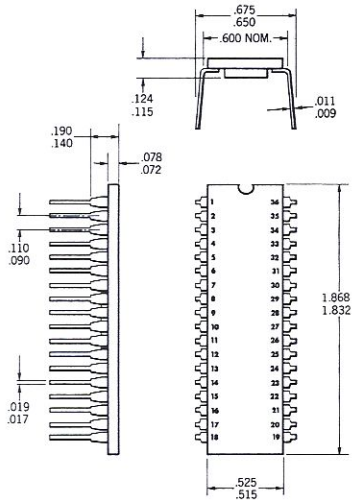
Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature (A6H380114X)	−55°C to +85°C
(A6H380119X)	0°C to +70°C

APPLICATIONS

Serial and Parallel Data Conversion in

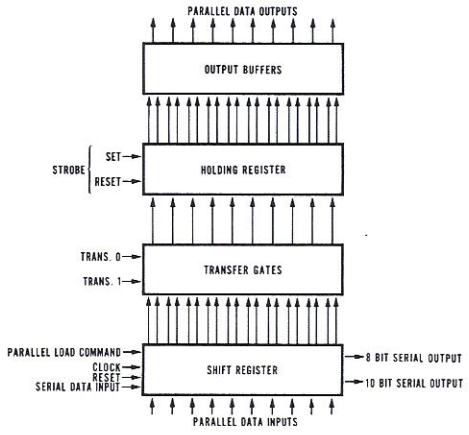
- Process Control
- Data Terminals
- Computer Peripheral Equipment
- Data Acquisition

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

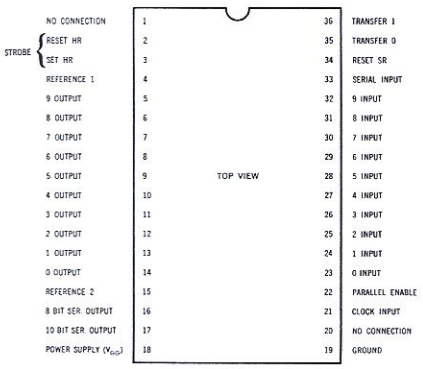


ORDER PART NO. A6H380114X
A6H380119X

BLOCK DIAGRAM



PIN CONFIGURATION



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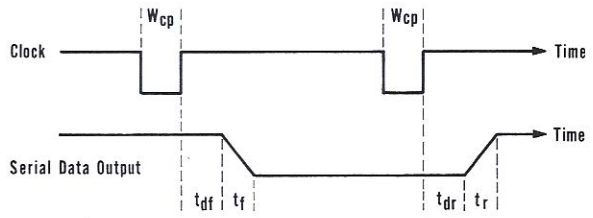
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10M\Omega$, $C_L = 10$ pF unless otherwise specified)

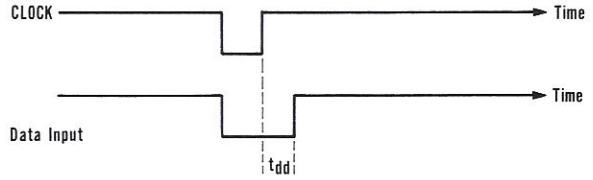
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10	−11		Volts	$R_L = 40$ kΩ
	"1"	−11	−12		Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TIMING DIAGRAM

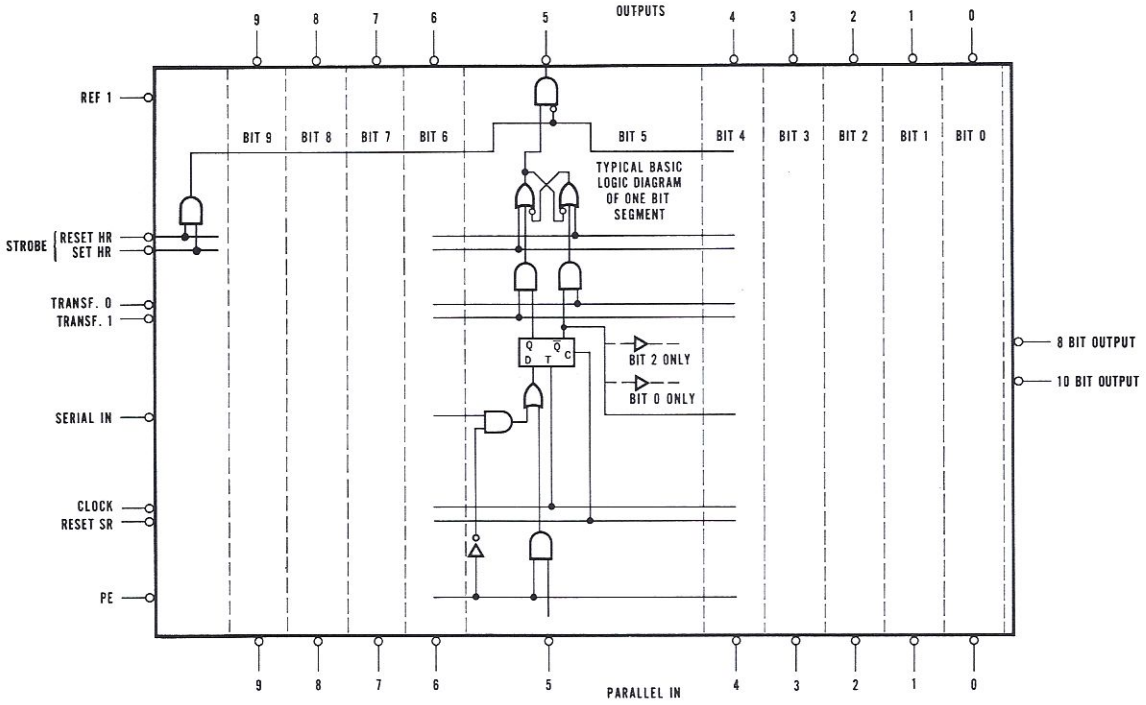
OUTPUT DELAY, RISE AND FALL TIMES



DATA BIT TIMING

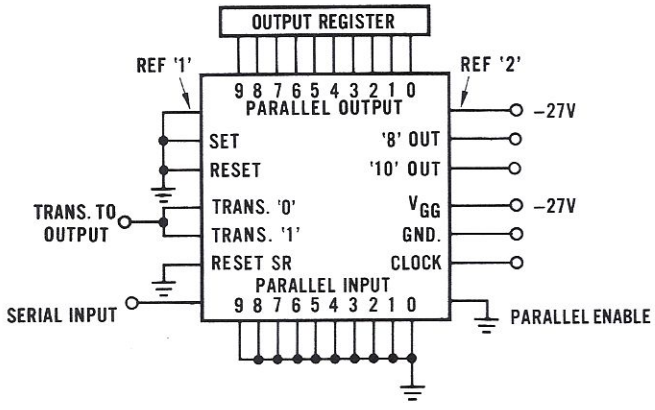


LOGIC DIAGRAM

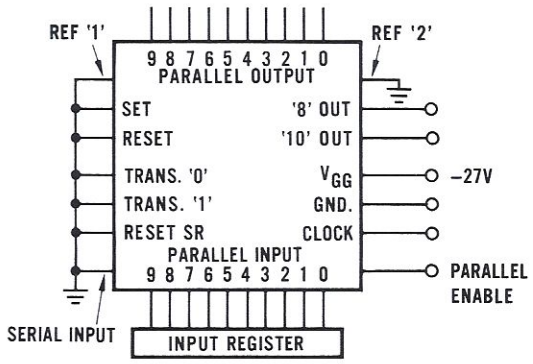


APPLICATIONS (Basic Logic Representation)

SERIAL TO PARALLEL CONVERTER



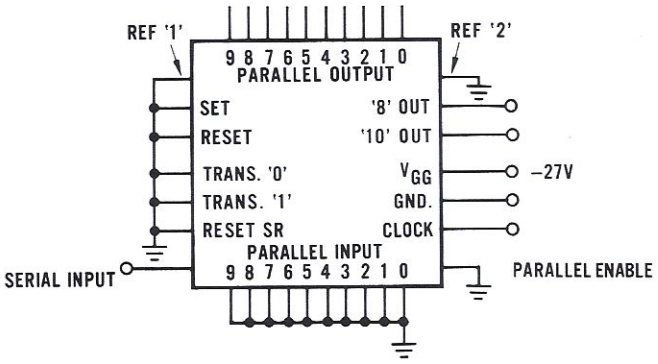
PARALLEL TO SERIAL CONVERTER



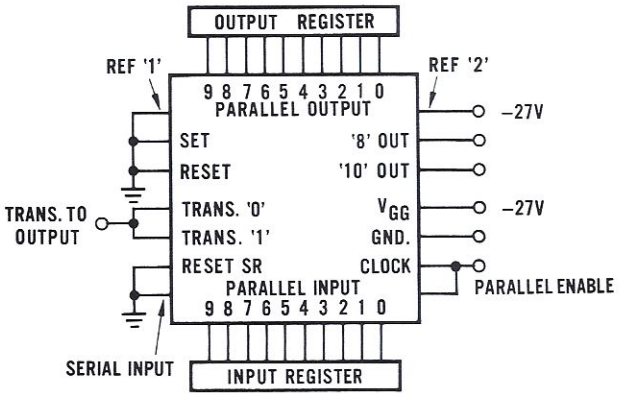
APPLICATIONS

(Basic Logic Representation)

SERIAL TO SERIAL BUFFER REGISTER



PARALLEL TO PARALLEL BUFFER REGISTER



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